Single-Crystal-Silicon Continuous Membrane Deformable Mirror Array for Adaptive Optics in Space-Based Telescopes

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***Abstract*—In this paper, we present a single-crystal-silicon (SCS) continuous membrane deformable mirror (DM) as a corrective adaptive-optics (AO) element for space-based telescopes. In order to correct the polishing errors in large aperture ($\sim$8 m) primary mirrors, a separate high-quality surface DM array must be used. Up to 400 000 elements and a mirror stroke of ~ 100 nm are required for the correction of these polishing errors. A continuous membrane mirror formed by the the SCS device layer of a silicon-on-insulator (SOI) wafer is used to achieve a high-quality optical surface and to minimize the additional diffractive effects in the optical system. To achieve substantial local deformation needed to correct high-order errors, we use a highly deformable silicon membrane of 300-nm thickness. This thin membrane is able to deform locally by 125 nm at an operating voltage of 100 V with a pixel pitch of 200 μm. The resonance frequency of a pixel is 25 kHz with a low Q-factor of 1.7 due to squeeze-film damping. The device is fabricated by processing the microelectromechanical system (MEMS) and electronic chips separately and then combining them by flip-chip bonding. This allows optimization of the MEMS and electronics separately and also allows the use of an SOI layer for the mirror by building the MEMS bottom up. A small prototype array of 5$\times$5 pixels with 200-μm pitch is fabricated, and we demonstrate single pixel and multiple pixel actuation.**

***Index Terms*—Adaptive optics (AO), continuous membrane, microelectromechanical system (MEMS), micromirror array, microoptoelectromechanical system (MOEMS), piston actuator, single-crystal-silicon (SCS), silicon-on-insulator (SOI), space telescope.**

I. INTRODUCTION

In this paper, we present a single-crystal-silicon (SCS) continuous membrane deformable mirror (DM) array with electrostatic actuation for applications in adaptive optics (AO) [1], [2]. AO used to correct the atmospheric distortion requires large strokes of up to several micrometers. For vision science applications, microelectromechanical system (MEMS) mirrors with strokes even higher than 10 μm are required. In space-based telescopes, where atmospheric distortion is a nonissue, imperfections of the optical system are the main cause of image degradation. Such optical systems require only short-stroke AO to correct the imperfections such as local defects of a few nanometers, large curvature flaws of several hundred nanometers, and component misalignment. For these types of corrections, the continuous face-sheet mirrors as described in this paper, perform better than the segmented mirrors that degrade the image quality through attenuation and diffraction.

The search for Earth-like planets (ELPs) using a space telescope, requires the wavefronts at the detector to be corrected to an rms error of $\sim\lambda/3000$ [3]. This is ~ 0.16 nm rms wavefront error at a center wavelength of $\lambda = 500$ nm. Such low wavefront error demands the optics to be of near perfect quality in terms of flatness and surface roughness. Image degradation in space-based telescopes is due to imperfections in the optical system, mainly in the primary and secondary mirrors. In order to resolve ELPs, the primary mirror must be of at least 8 m in diameter. Current polishing technology cannot polish mirrors of this size to the required specifications, so the residual error must be corrected with additional optics, e.g., a MEMS deformable mirror (DM). In polishing the primary mirror, there are roughly concentric polishing errors of up to ~ 300 cycles/aperture. These concentric polishing errors of n cycles/aperture act as coarse gratings and diffract light to n Airy radii. This diffracted light will blur the faint ELP next to a very bright star. Although using concentric mirror elements would allow significant reduction of the number of elements and improve the surface error substantially, this approach will not fully correct for the errors to the required specifications. The polishing errors are expected to be in the range of 30 to 100 nm in peak-to-valley amplitude, and so, the mirror array must be able to deflect up to 100 nm. It is expected that an 8-m class telescope requires a DM of ~ 400000 mirrors of high surface quality. The roughly concentric polishing errors should be ~ 312 cycles/aperture, and using two sampling points per cycle in two dimensions results in $(2\times 312)^2 = \sim 400000$ actuators. For this application, bulky AO-DMs made with large stroke capable actuators are costly to fabricate and deploy [4]. MEMS-DMs allow scalability, repeatability, and low fabrication cost of $\sim\$1$ per actuator. In order to achieve a sufficiently high-quality optical surface, we utilize a silicon-on-insulator (SOI) device layer for the continuous membrane mirror. The mirror is also a continuous membrane to minimize the diffractive effects. Although the membrane is very thin, the stroke required is small compared to the thickness. Otherwise, the thin membrane, if required to change many times its thickness, will encounter fatigue and fracture. The speed of the device is not an issue,

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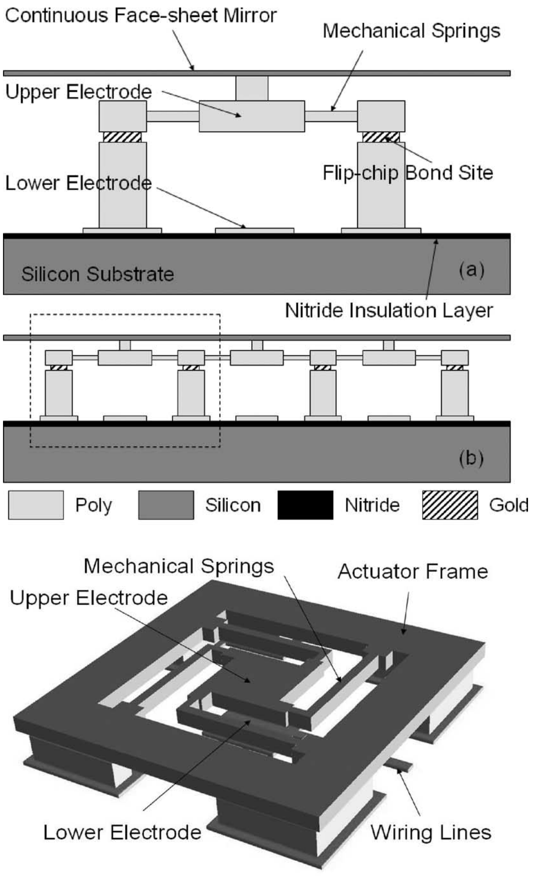


(c)

Fig. 1. Diagram of a continuous membrane DM. (a) Single pixel. (b) Array. (c) Volume model of the actuator.

since unlike AO elements for ground-based telescopes, there is no continuously varying atmospheric turbulence to compensate. Hence, the resonance frequency of the device may be omitted from consideration in the design. More important is the accuracy and stability of the device. The stroke actuation must be very accurate for the correction of polishing errors, and stability is important because the DM is set to correct the residual polishing errors on the primary mirror and then, must remain in that state continuously over long period of time.

II. DESIGN

Our approach to the fabrication of a continuous membrane MEMS mirrors differ from earlier reported methods [4]–[7], in that we fabricate the electronics and MEMS on different wafers and combine these with flip-chip bonding [8]. The advantage of this approach is that the MEMS and electronics can be optimized independently and separate foundries can be used. In particular, the electronics can be made in a standard foundry without the extra complexity that is associated with direct integration of MEMS. This method also allows the fabrication of the top membrane using a sufficiently flat low-stress SCS device layer.

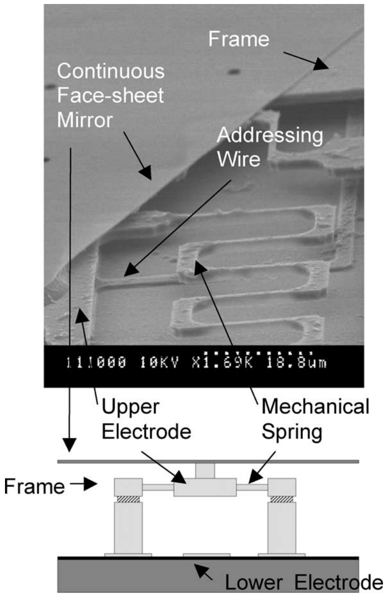


Fig. 2. SEM showing the actuator structure of a single pixel.

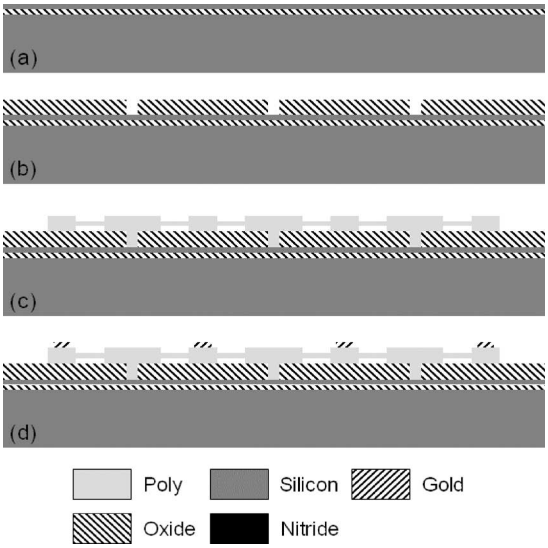


Fig. 3. Process flow diagram of the MEMS chip.

Fig. 1 shows the structure of the DM. Fig. 1(a) shows the cross-sectional view of a single pixel and Fig. 1(b) shows three elements of an array. Fig. 2 shows a SEM of the structure. The thin membrane is attached to the actuator through a via connection from the actuator poly layer. This via (or post) is connected to the upper electrode plate. This electrode plate is connected to the stationary frame by four serpentine springs. The springs and upper electrode plate have various designs from simple straight springs to curved springs that maximize the area of the circular electrodes. The frame is offset from the lower electrode layer by polysilicon and gold layers. The upper electrode, membrane, and spring structures are all at the ground potential, and the bottom electrodes are individually addressed for applying voltage. The center of the membrane is pulled down by parallel-plate actuation when voltage is applied between the upper electrode plate and the lower electrode plate. In order to simplify fabrication, the addressing wires are made in the same layer as the lower electrodes and run underneath other pixels which may cause some crosstalk. Simulations show that this effect is negligible.

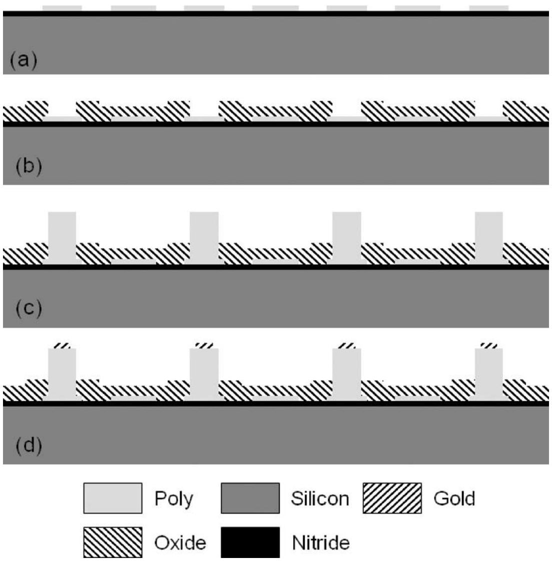


Fig. 4. Process flow diagram of the electrode chip.

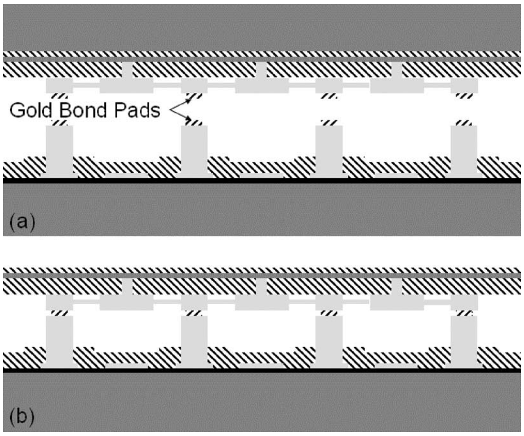
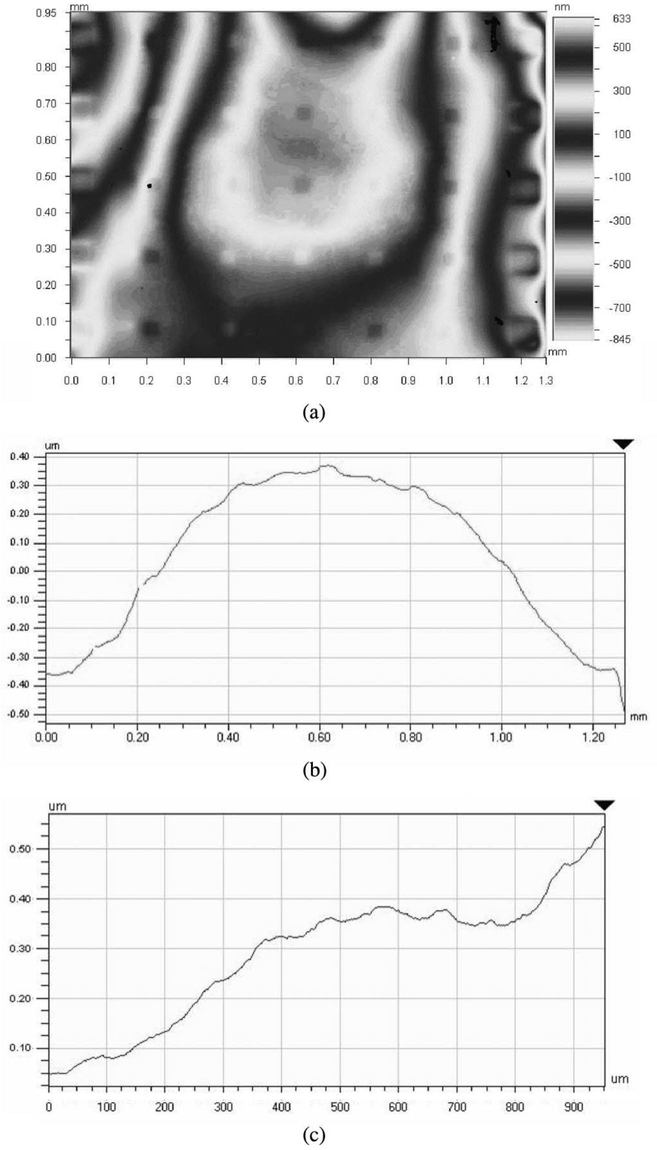


Fig. 5. (a) Flip-chip bonding. (b) Upper substrate release by XeF_2.

III. FABRICATION

In order to facilitate the use of a SCS device layer for the continuous membrane mirror, the fabrication for the MEMS and electronics wafer is done separately. For the MEMS chip fabrication (Fig. 3), the top membrane is a 300-nm SOI device layer with a buried oxide (BOX) of 500 nm. This layer is patterned to define the aperture of the membrane with some of the chips having small holes in the membrane to help with release. A 2.0-μm-thick phosphorous-silicate-glass (PSG) is deposited to define the height of the post that connects the upper membrane to the upper electrode of the actuator. This is patterned to form the vias that are filled with polysilicon to form the post. Then, a 2.0-μm-thick polysilicon layer is deposited and patterned to form the post, upper electrode, springs, and the upper frame of the actuator. The upper electrodes have a reduced effective area due to the conformal deposition dip in the center that forms the post to the upper SOI membrane. The wafer is then annealed at 1000 °C for 1 h to dope the polysilicon layer from the PSG layer. A gold layer of 500 nm is patterned by liftoff to form flip-chip bond pads.



(a)

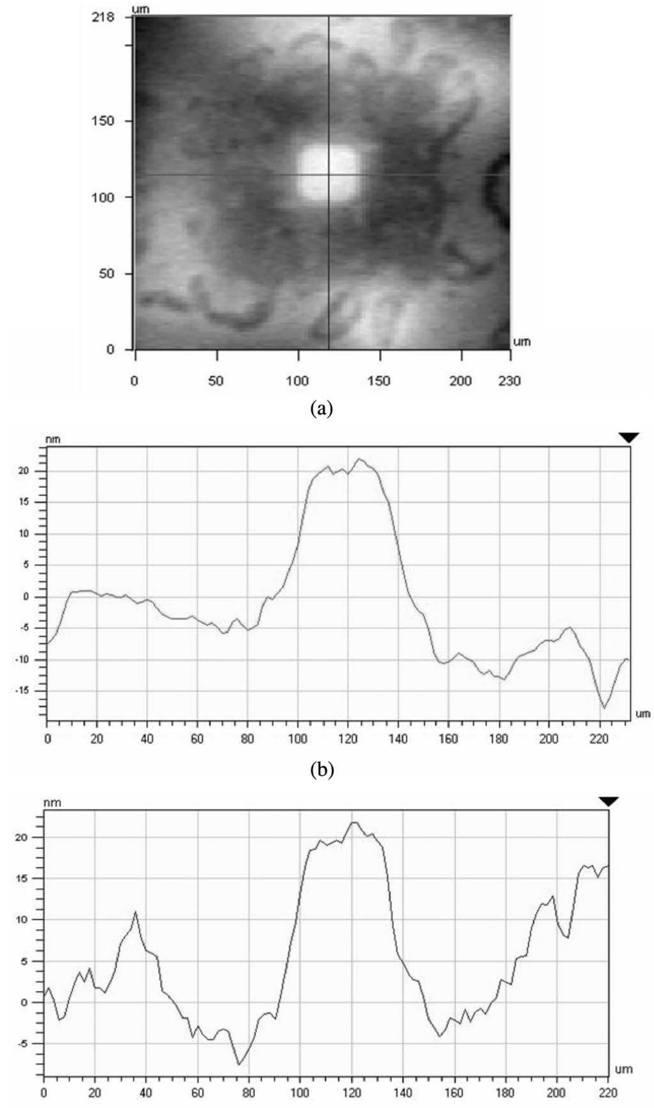
(b)

(c)

Fig. 6. (a) Optical surface profile of the continuous membrane and cross-sectional plots across the center of membrane in (b) X and (c) Y.

The electronics chip fabrication as shown in Fig. 4, starts with the deposition of a 600-nm nitride insulation layer. We will use the term "electronics chip" even though no actual electronics are built in our chip. A 500-nm layer of polysilicon is deposited to form the addressing lines, base of the offset structures, and the lower electrodes. Then, a 0.5-μm PSG is deposited and patterned to create vias for the offset structures and to dope the lower electrodes. A polysilicon layer of 2.0 μm and 300 nm of PSG is deposited and annealed at 1000 °C for 1 h. The 300-nm PSG layer is stripped, and then the poly layer is patterned to form the offset "leg" structures. The offset structure also acts as an electrical connection to the upper electrodes and membrane which is electrically grounded. Finally, a gold layer of 500 nm is patterned by liftoff to form the flip-chip bond pads.

The MEMS chip and electronics chip were flip-chip bonded (see Fig. 5) using a research devices manual bonder at 300 °C under 1 kg of pressure. Release of the upper substrate was done



(a)

(b)

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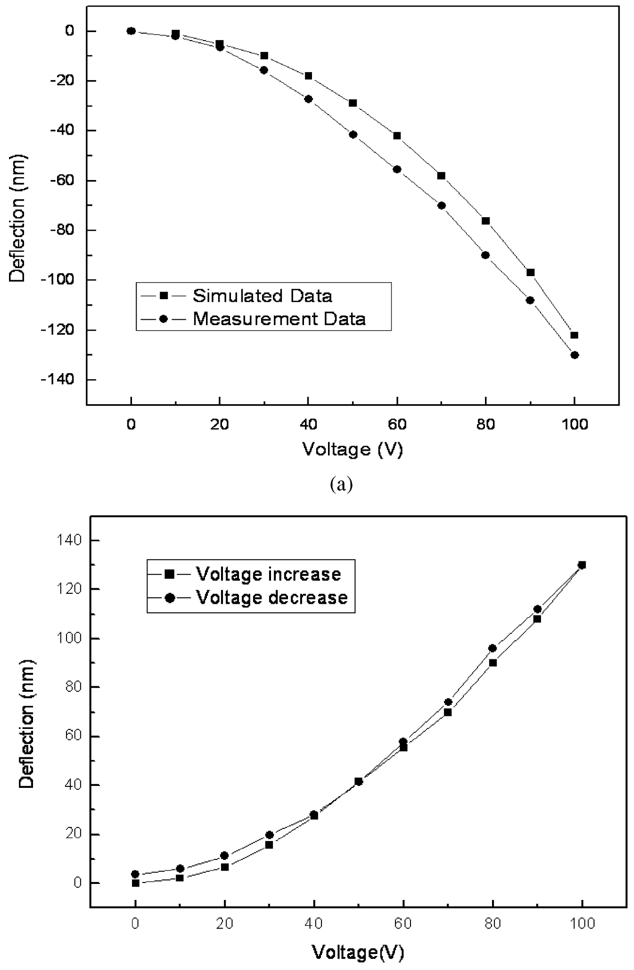
Fig. 7. (a) Surface profile of a single pixel with the center bump and cross-sectional profiles across the center in (b) X and (c) Y.

using a XeF_2 etcher. The XeF_2 etch is isotropic and can etch between the chips, so, protection of the other areas is critical. We use black wax to protect the sides and gaps in between the upper and lower chips and to mount them to pyrex wafers for etching. Although it is an isotropic etch, the etching itself is fairly anisotropic due to the wax, which acts as a guiding etchstop on the walls. The wax is removed with solvents, and the oxide is released in concentrated hydrofluoric acid (HF). Finally, the chips are dried in a critical point dryer (CPD). This is a very critical step due to the thin membrane layer. Careful handling during the wet oxide release and subsequent rinsing in water and solvents is crucial for the yield of working devices.



(a)

(b)

Fig. 8. (a) Static deflection measurement and simulated data. (b) Static deflection curve showing hysterisis.

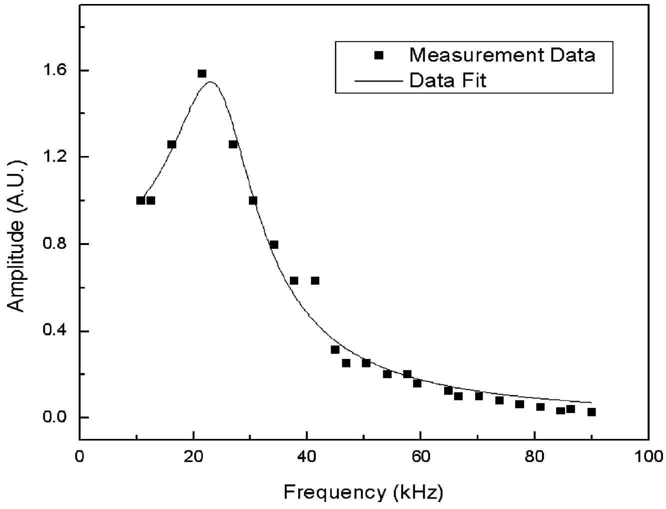
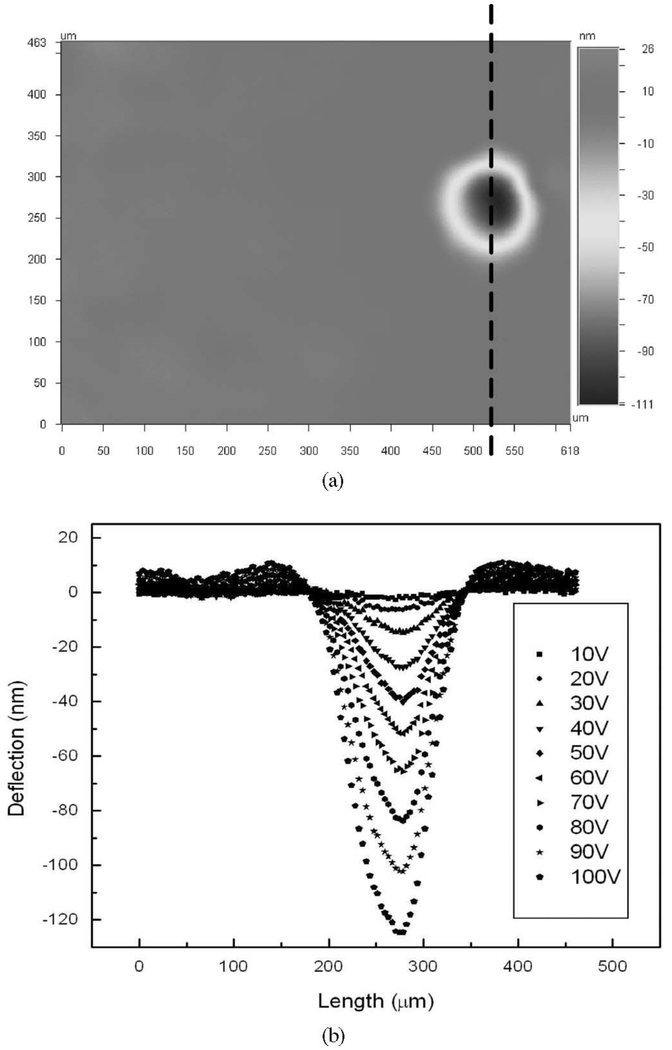


Fig. 9. Frequency response measurement.

IV. DEVICE CHARACTERIZATION

The surface profile of the mirror array measured with a Wyko optical profiler is shown in Fig. 6(a). The center 1.0 mm × 1.0 mm area has a 5 × 5 array of active pixels with a pitch of 200 μm. The outer two columns have dummy pixels that bound and support the upper membrane. The radius of curvature of the unactuated mirror is 0.23 m in the x-direction [Fig. 6(b)]. The y-direction profile has a single peak and valley



(a)

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Fig. 10. (a) Surface profile of a single pixel actuated at 90 V. (b) Cross-sectional profiles of a single pixel actuation.

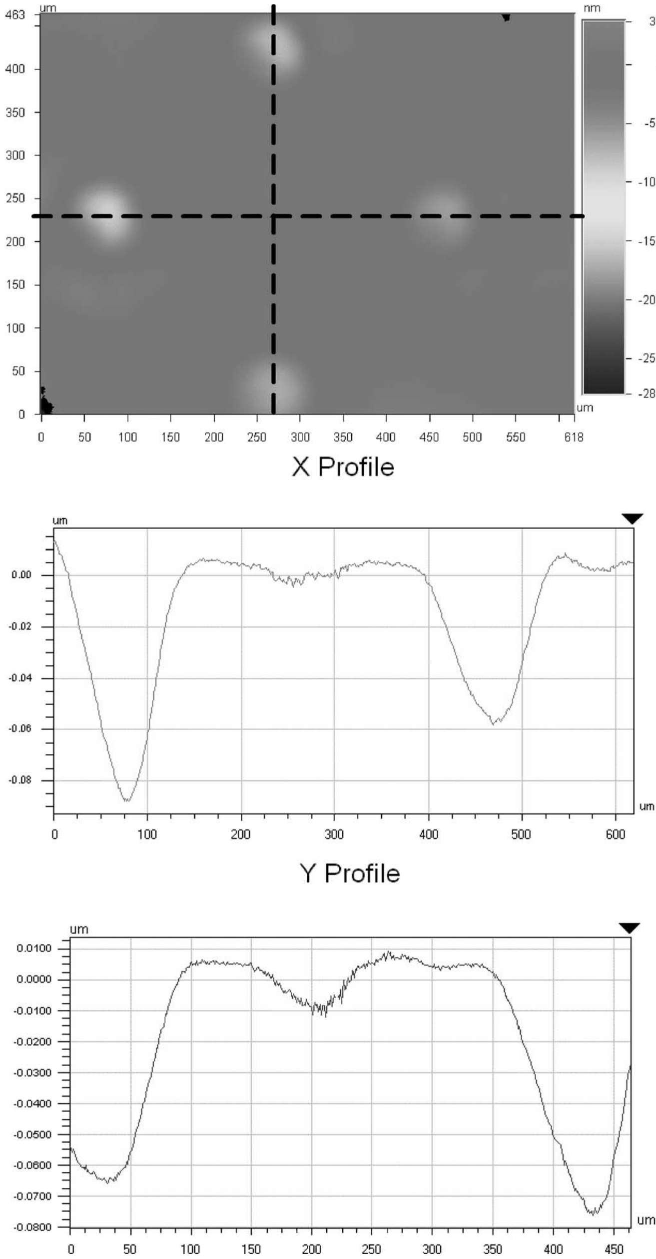

Fig. 11. Surface profile and cross-sectional profiles of multiple pixels actuated at 80 V.

with a difference of ~100 nm with the tilt removed [Fig. 6(c)]. Stress in the poly actuator layer is believed to be the cause of the curvature. This may be resolved using a nitride/poly actuator layer to compensate for the stresses. The total surface roughness of the array with the curvature term removed is 19 nm. The largest contribution to the roughness is the pedestal attachment to the upper membrane [Fig. 7(a)], which causes a bump in the membrane with a height of ~25 nm [Fig. 7(b) and (c)]. The single pixel area surface roughness is 9-nm rms, which is mainly due to the post attachment.

Static deflection measurements show that the membrane deforms ~125 nm in the center at 100 V [Fig. 8(a)] and closely matches simulated data. Fig. 8(b) shows the hysterisis curve of a single pixel actuated up to 100 V and back to 0 V. Although there is no significant difference in the middle of the curve where hysterisis is usually prominent, the pixel does have a noticeable difference back in the initial state. Fig. 9 shows the frequency response of a pixel measured using a fiber-interferometer and spectrum analyzer. The actuators were driven at 60 sin ωt V using an Intellite high-voltage MEMS driver and function generator. The measurement showed a resonance frequency of 25 kHz and a Q of 1.7. This is close to the simulated value of 27 kHz for the fundamental piston mode. The relatively low Q is expected to be due to squeezed-film damping of the large area continuous membrane of 1 mm with a small gap of 2 μm.

Fig. 10 shows the surface profile and the cross section of a pixel under varying potential. The plot is a differential measurement between the profiles at a certain voltage and the profiles at 0 V. This is done to enhance the visualization of the deformation, as the deflections are small compared to the curvature of the membrane area. The plot shows that at 200-μm pitch, there is less than 10% crosstalk such that the deformation is localized within the pitch. Fig. 11 shows several pixels in a checkerboard configuration being actuated at 80 V. Three pixels show similar deflections with one pixel having a slightly larger deflection than the others. This may be due to the initial state where this pixel has a smaller initial gap after release. The center dip in Fig. 11(b) and (c) in the nonactuated center pixel can be attributed mainly to the address wires of other pixels running underneath this pixel.

V. CONCLUSION

We have designed and fabricated an SCS continuous membrane DM array with a 300-nm-SOI device layer. This type of device can be scaled with varying membrane thickness to be optimized for specific ranges in deformation from a few nanometers to micrometers, as required by specific AO applications. For the application of correction of polishing errors in space-based telescopes, we have designed and fabricated a prototype 5×5 mirror array that has a pitch of 200 μm and a surface roughness of 19 nm. The reduced surface quality of the mirror is mainly from the stressed polysilicon post attachment and the initial curvature caused by the stress in the actuator. A reduced post area and use of stress-compensated films may reduce these problems for better results. A pixel is capable of localized deformation of $\sim$125 nm at 100 V with minimal crosstalk. We show the deformations to have good profiles and also show the multiple pixel actuation with relatively uniform deformation characteristics between the pixels. These devices are designed for wavefront correction in simple open-loop optical systems. With improved initial surface quality of the membrane and increased number of actuators for the specification, we expect that this type of device can be used to correct the polishing errors of small amplitudes, in order to effectively improve the surface quality of the primary mirror in space-based telescopes.

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