7 Summary of Adaptive Optics at Stanford

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Summary. The status of adaptive optics at Stanford is summarized. Particular focus is given to the fabrication and testing of segmented, micro-mirror SLMs developed under the CCIT (Coherent Communications, Imaging, and Targeting) project [1]. Square and hexagonal "5×5" and "32×32" arrays have been fabricated using MEMS technology, and "5×5" arrays have been characterized.

7.1 Introduction

For the past two years, the development of wavefront correction technology at Stanford has supported the CCIT (Coherent Communications, Imaging, and Targeting) project [1]. Funded by DARPA, its main objective is to develop a million-pixel mirror array capable of piston and tip/tilt motions and associated packaging and electronics. The principal participants in this project are the Lawrence Livermore National Laboratory (electronics and testing), MicroAssembly Technologies (packaging), Lucent Technologies (packaging and testing), Boston University (fabrication and testing), Boston Micromachines (fabrication and testing), and Stanford University (fabrication and testing).

Potential applications of these mirror-based spatial light modulators include secure free space communication, aberration correction for lasers, astronomy, ophthalmology, nano-scale manipulations of particles, projection displays, and maskless photolithography.

Table 7.1 summarizes the requirements of the CCIT project.

7.2 History of CCIT Mirror Development at Stanford

The program milestones included the development of piston-only mirrors prior to the fabrication of mirrors capable of piston motion in combination with rotation on two orthogonal axes (tip/tilt motion). The first generation micro-mirror piston SLMs developed for the CCIT project at Stanford [2] used a commercial MEMS process called MUMPs® [3, 4]. Mirror and electrode chips were made in parallel and integrated via flip-chip bonding. This permits separate optimization of mirrors and electrodes and prevents print-through of electrode patterns on the mirror surface.

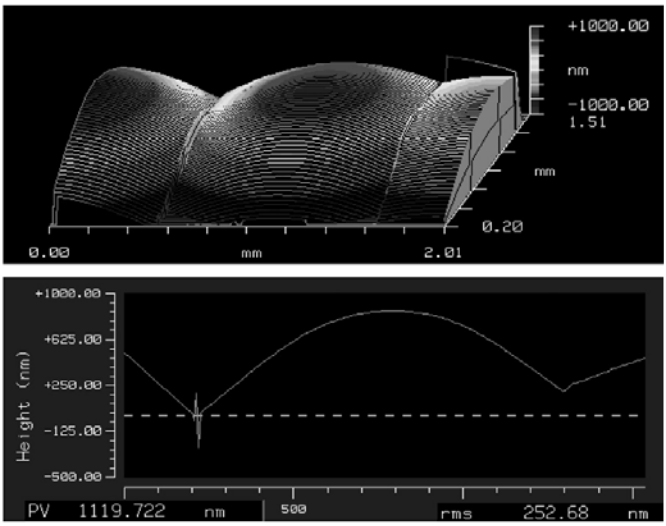

Fig. 7.1. One MUMPs mirror measured using an interferometric profilometer. The height between the center and the edge due to stress is greater than one micron

Though the convenience of having a commercial foundry complete most of the fabrication steps offers a compelling reason to use MUMPs, the flatness requirements of the project were not met. Under MUMPs, mirror surfaces were made of polysilicon, which was deposited with small but finite stress gradients. After an HF release, these mirrors became highly curved. Figure 7.1 shows measurements made of an array completed using this process. The difference in mirror height between the center of a pixel and its edge is over one micron, which exceeds the target actuation depth of 0.75 µm.

Table 7.1. CCIT project requirements

Category	Requirement
Pixel size	100 µm × 100 µm
Pixel count	10^6
Pixel flatness	$\lambda/50$ at 1.5 µm, or 30 nm
Piston response time	$\leq$ 10 µs, or resonant frequency $>$ 100 kHz
Tip/tilt response time	$\leq$ 100 µs, or a resonant frequency $>$ 10 kHz
Fill factor	$>$ 98%
Piston stroke depth	$\lambda/2$ at 1.5 µm
Piston resolution	$\geq$ 8 bits or 256 levels, or 3 nm
Tip/tilt max deflection	$\pm 10^\circ$ mechanical, or $\pm 20^\circ$ optical
Tip/tilt resolution	$\geq$ 10 bits or 200 µrad
Operating voltage	$\approx$ 100 V

7.3 SOI Process: Fabrication

An alternate process was developed to address mirror flatness based on SOI technology, which previously has been shown to yield devices with high surface quality [5, 6]. SOI wafers typically consist of a 500 µm silicon substrate and a 5–10 µm device layer separated by a micron of thermal oxide. Under this process, the device layer, composed of bulk silicon, becomes the mirror surface. This leads to improved pixel flatness values that exceed the program specifications.

Like the MUMPs process, this new process involves flip-chip bonding. The procedure for fabricating mirror chips is as follows:

- Discrete mirror elements, or pixels, are patterned onto the device layer of an SOI wafer using a Deep Reactive Ion Etch (DRIE) based on the Bosch process (Fig. 7.2).
- A one micron layer of low-temperature oxide is then deposited using Low-Pressure Chemical Vapor Deposition (LPCVD). This is a sacrificial layer which must be removed later.
- Next, a wet etch, using a 6 : 1 Buffered Oxide Etch (BOE), creates holes in the oxide directly over the center of each pixel.
- Then a 2 µm layer of amorphous silicon is deposited with another LPCVD. This layer will eventually become the actuator, or spring which bends and flexes to allow mirror motions.
- The actuator needs to be conductive, so 0.4 µm of phosphorous-doped oxide is deposited onto this layer, annealed for an hour, and then stripped. This allows for the diffusion of dopants into the amorphous silicon layer.
- Then, spring structures are patterned onto the amorphous silicon layer using a RIE (Fig. 7.3).
- Following this, gold bond pads are deposited at specific sites on the actuator. The gold bond pads of the mirror chip are then aligned to the gold pads of the electrode chip, and the two chips are pressed together at 100 MPa and heated to 300°C.
- Next, the silicon substrate is removed using either a XeF_2 or Bosch etcher.
- Then, 49% hydrofluoric acid (HF) is used to remove the sacrificial oxide layers, and a critical point drying procedure is performed.
- Finally, the array is wire-bonded (Fig. 7.5).

7.4 SOI Process: Fabrication Results

Arrays composed of hexagonal and square pixel elements were both fabricated. Hexagonal arrays had sizes of 19 and 1027 elements, and square arrays of 25 and 1024 elements. For convenience, the smaller arrays will be referred to as "5 × 5" and the larger ones as "32 × 32". The "5 × 5" arrays have been assembled and tested. Figure 7.6 shows that single pixels on a "5 × 5"

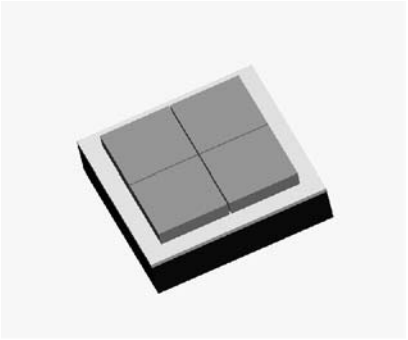

Fig. 7.2. *Top* and *bottom*: silicon device layer patterned with mirrors, oxide, silicon substrate

Fig. 7.3. Patterned actuators. The sacrificial oxide layer not shown

array were flat to within 2 nm as measured by a white-light interferometer, with 30 nm rms of roughness and one meter of curvature for the entire array. Figure 7.7 shows a static actuation measurement made of a square "5×5" array. A half-wavelength of displacement was achieved at 80 V. Based on the observed spring constant, the resonant frequency is calculated to be 80 kHz. Square pixels are 200 µm in size while hexagonal pixels are 300 µm. The gap between mirrors is 2 µm. This corresponds to a fill factor of over 99%.

The "32×32" arrays have been fabricated, though with less reliability than the "5×5" arrays. Frequently, the mirror and electrode chips become debonded after the substrate is removed, possibly because of stress between the Si and SiO_2 layers producing lateral shear forces on the gold to gold bond junction. This stress does not cause problems in "5×5" arrays, but becomes increasingly significant when array sizes are scaled upwards.

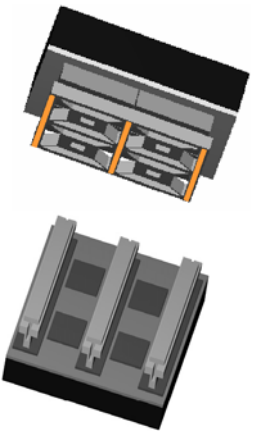

Fig. 7.4. Top and bottom chips ready for bonding

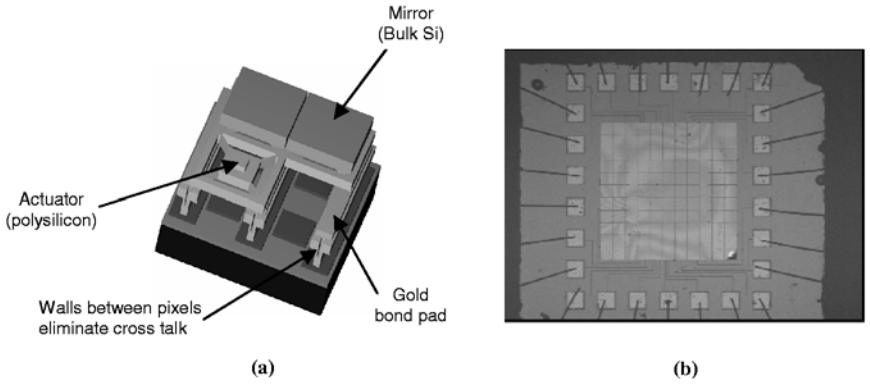

Fig. 7.5. (**a**) 3-D model of completed array. (**b**) Square "5×5" array–wire-bonded and surrounded by dummy pixels (total 11×11)

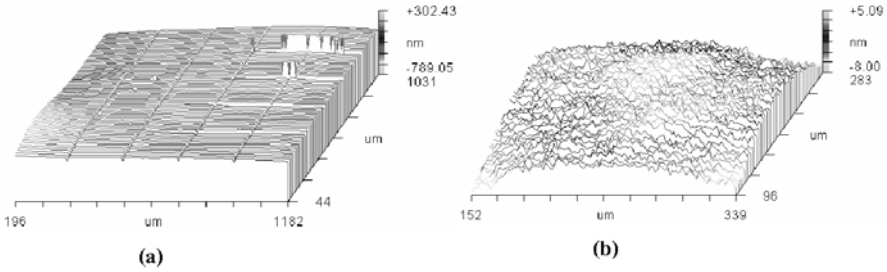

Fig. 7.6. (**a**) Flatness measurements of an SOI-process array. (**b**) Measurements of a single pixel

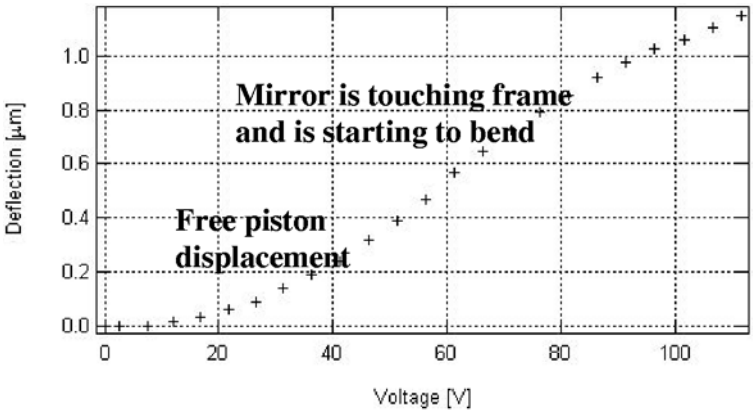

Fig. 7.7. Static actuation measurement of a pixel in a "5 × 5" array

7.5 Future Work

Work pertaining to the "32 × 32" arrays involves increasing fabrication reliability and characterizing previously fabricated devices. A possible solution to the debonding problem mentioned above is to partially remove the substrate prior to performing the HF release, leaving behind a grid pattern. This would lend structural support to the mirrors on the opposing side of the oxide membrane. Investigations of this approach are in progress.

The next major thrust of CCIT is the fabrication of mirrors capable of tip, tilt, and piston motions. Designs and simulations for these mirrors, based on a dual-gimbaled vertical comb drive structure, have been completed.

Another area of future work would be the inclusion of piston-only mirrors in laser-power scaling experiments. For these, segmented mirrors will be placed in a laser Master Oscillator Power Amplifier (MOPA) configuration where the phase of a beam is pre-corrected prior to sending it through slab amplifiers. Since the incident power on these mirrors will be on the order of watts, power absorbed in the gaps between the mirrors will not be significant.

Another application for these segmented mirrors is to create a supermode from a phased array of laser beamlets. The phase of each beamlet in the supermode is to be independently controlled by a pixel in the array. This will permit coherent far-field adding of the beamlets and active beam steering.

7.6 Conclusion

Using the MUMPs process for fabricating micro-mirror arrays produced curved mirrors where peak to valley distortions exceeded the target stroke depth of 0.75 µm. Another flip-chip bonding process, involving SOI technology, was developed to solve this problem. Square and hexagonal "5×5" arrays

were assembled using the SOI process in Stanford clean rooms and characterized. These mirrors, made from the device layer of SOI wafers, have individual pixels which are flat to within 2 nm. The fabrication of "32 × 32" arrays is being optimized, and existing "32 × 32" devices will soon be characterized. Finally, tip/tilt/piston mirrors have been designed and their fabrication is underway.

Acknowledgements

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